What is claimed is:

1. A circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, including:

first circuitry coupled to receive the input clock and configured to generate a control signal indicative of events having time-averaged frequency at least nearly equal to $(A/T)F_i$, where A and T are integer values, such that accumulated error, between a first time from a first one to a last one of Z consecutive ones of said events and a second time equal to $ZT/(AF_i)$, never exceeds $1/F_i$; and

second circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal such that leading edges of the pulses occur at least nearly periodically, with said time-averaged frequency at least nearly equal to $(A/T)F_i$, and with accumulated error, between a third time from a first one to a last one of Z consecutive ones of said leading edges and the second time $ZT/(AF_i)$, that never exceeds $1/F_i$.

2. The circuit of claim 1, wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to increase the Count value by the value A during each cycle of the input clock; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value T during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value T – A when the output signal indicates that the Count value has risen to a value greater than or equal to said value T, and wherein the output signal is said control signal.

3. The circuit of claim 2, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to reset the Count value to an initial value I whenever the frame start signal is indicative of one of the frame start events.

4. The circuit of claim 3, wherein the initial value I is equal to zero.

5. The circuit of claim 4, wherein the second circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has risen to said value greater than or equal to said value T.

6. The circuit of claim 5, wherein the logic circuitry is configured to assert each of the sync pulses with any selected one of at least two different pulse widths.

7. The circuit of claim 5, wherein the frame start events occur with a first phase, and the logic circuitry is configured to assert the sync pulses so that their leading edges have any selected one of at least two different phases relative to said first phase.

8. The circuit of claim 4, wherein the second circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses having a first width whenever the frame start signal is indicative of one of the frame start events, and to assert one of the sync pulses having a second width whenever the output signal indicates that the Count value has risen to said value greater than or equal to said value T, wherein the first width is different than the second width.

9. The circuit of claim 8, wherein the first width is greater than the second width, and the logic circuitry is configured to set each of the first width and the second width to be any selected one of a set of at least two different pulse widths.

10. The circuit of claim 1, wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to increase the Count value by the value A during each cycle of the input clock; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value T during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value T– A when the output signal indicates that the Count value has risen to a value greater than said value T, and wherein the output signal is said control signal.

11. The circuit of claim 10, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to reset the Count value to an initial value I whenever the frame start signal is indicative of one of the frame start events.

12. The circuit of claim 11, wherein the initial value I is equal to zero, the second circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has risen to said value greater than said value T.

13. The circuit of claim 1, wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to decrease the Count value by the value A during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + T, whenever the frame start signal is indicative of one of the frame start events, where X is a value and T is an integer value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value T – A when the output signal indicates that the Count value has fallen to a value less than or equal to said value X, and wherein the output signal is said control signal.

14. The circuit of claim 13, wherein the second circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has fallen to said value less than or equal to said value X.

15. The circuit of claim 1, wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to decrease the Count value by the value A during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + T, whenever the frame start signal is indicative of one of the frame start events, where X is a value and T is an integer value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value T – A when the output signal indicates that the Count value has fallen to a value less than said value X, and wherein the output signal is said control signal.

16. The circuit of claim 15, wherein the second circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has fallen to said value less than said value X.

17. A circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, including:

an accumulator configured to store a Count value, and to increase the Count value by an integer value D during each cycle of the input clock;

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with a threshold value N during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison, wherein N is an integer, wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value N – D when the output signal indicates that the Count value has risen to a value greater than or equal to said value N; and

pulse generation circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal.

18. The circuit of claim 17, wherein the pulse generation circuitry is configured to generate the sync pulses such that leading edges of the sync pulses occur with accumulated error, between a time from a first one to a last one of Z consecutive ones of said leading edges and a second time equal to $ZN/(DF_i)$, that never exceeds $1/F_i$.

19. The circuit of claim 17, wherein said circuit is a field-programmable gate array.

20. The circuit of claim 17, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to reset the Count value to an initial value I whenever the frame start signal is indicative of one of the frame start events.

21. The circuit of claim 20, wherein the initial value I is equal to zero.

22. The circuit of claim 20, wherein the pulse generation circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has risen to said value greater than or equal to said value N.

23. A circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, including:

an accumulator configured to store a Count value, and to increase the Count value by an integer value D during each cycle of the input clock;

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with a threshold value N during each cycle of the

input clock and to generate an output signal indicative of the result of each said comparison, wherein N is an integer, wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value N – D when the output signal indicates that the Count value has risen to a value greater than said value N; and

pulse generation circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal.

24. The circuit of claim 23, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, the accumulator is configured to reset the Count value to an initial value I whenever the frame start signal is indicative of one of the frame start events, the initial value I is equal to zero, and the pulse generation circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has risen to said value greater than said value N.

25. A circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, including:

an accumulator configured to store a Count value, and to decrease the Count value by an integer value D during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + N, whenever the frame start signal is indicative of one of the frame start events, where X is a value and N is an integer value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input clock and to generate an output signal indicative of the result of each said

comparison, wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value N – D when the output signal indicates that the Count value has fallen to a value less than or equal to said value X; and

pulse generation circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal.

26. The circuit of claim 25, wherein the pulse generation circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has fallen to said value less than or equal to said value X.

27. A circuit for generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, including:

an accumulator configured to store a Count value, and to decrease the Count value by an integer value D during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + N, whenever the frame start signal is indicative of one of the frame start events, where X is a value and N is an integer value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison, wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value N – D when the output signal indicates that the Count value has fallen to a value less than said value X; and

pulse generation circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal.

28. The circuit of claim 27, wherein the pulse generation circuitry is logic circuitry coupled to receive the output signal and the frame start signal, and configured to assert one of the sync pulses whenever the frame start signal is indicative of one of the frame start events, and whenever the output signal indicates that the Count value has fallen to said value less than said value X.

29. A system for generating a video signal, including:

a TV encoder having an output;

graphics processing circuitry coupled to the clock generator and the TV encoder, and configured to clock out frames of image data to the TV encoder in response to an input clock having frequency F_i, wherein the TV encoder is configured to generate a video signal in response to the image data and to clock out pixels of the video signal to the output in response to an output clock; and

a sync generator circuit coupled and configured to generate a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to the input clock, wherein said sync generator circuit includes:

first circuitry coupled to receive the input clock and configured to generate a control signal indicative of events having time-averaged frequency at least nearly equal to $(A/T)F_i$, where A and T are integer values, such that accumulated error, between a first time from a first one to a last one of Z consecutive ones of said events and a second time equal to $ZT/(AF_i)$, never exceeds $1/F_i$; and

second circuitry coupled to receive the control signal and configured to assert the sync pulses in response to said control signal such that leading edges of the pulses occur at least nearly periodically, with said time-averaged frequency at least nearly equal to $(A/T)F_i$, and with accumulated error, between

a third time from a first one to a last one of Z consecutive ones of said leading edges and the second time $ZT/(AF_i)$, that never exceeds $1/F_i$.

30. The system of claim 29, wherein the output clock has frequency XF_o, X is an integer, and the frequency F_i is equal to $(T/A)F_o$, and wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to increase the Count value by the value A during each cycle of the input clock; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value T during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value T – A when the output signal indicates that the Count value has risen to a value greater than or equal to the value T, and wherein the output signal is said control signal.

31. The system of claim 30, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to reset the Count value to an initial value I whenever the frame start signal is indicative of one of the frame start events.

32. The system of claim 31, wherein the initial value I is equal to zero.

33. The system of claim 31, wherein there are ICPOL cycles of the input clock per line of the video signal, where ICPOL = ICPIL * ILPIFRM * 2/ OLPOFRM, where ICPIL is the number of input clock cycles per line of the image data, ILPIFRM is the number of lines of the image data per frame of the image data, and OLPOFRM is the number of lines of the video signal per frame of said video signal, and wherein the value T is equal to ICPIL * ILPIFRM * 2 ,

and the value A is equal to OLPOFRM.

34. The system of claim 31, wherein there are ICPOL cycles of the input clock per line of the video signal, where ICPOL = ICPIL * ILPIFRM / OLPOFRM, where ICPIL is the number of input clock cycles per line of the image data, ILPIFRM is the number of lines of the image data per frame of the image data, and OLPOFRM is the number of lines of the video signal per frame of said video signal, and wherein the value T is equal to ICPIL * ILPIFRM, and the value A is equal to OLPOFRM.

35. The system of claim 31, wherein there are ICPOL cycles of the input clock per line of the video signal, where ICPOL = ICPIL * ILPIFRM / (2*OLPOFRM), where ICPIL is the number of input clock cycles per line of the image data, ILPIFRM is the number of lines of the image data per frame of the image data, and OLPOFRM is the number of lines of the video signal per frame of said video signal, and wherein the value T is equal to ICPIL * ILPIFRM, and the value A is equal to (2*OLPOFRM).

36. The system of claim 31, wherein the sync generator circuit is configured to be operable in any selected one of multiple operating modes.

37. The system of claim 36, wherein the operating modes include a first mode and a second mode, wherein

in the first mode, there are ICPOL cycles of the input clock per line of the video signal, where ICPOL = ICPIL * ILPIFRM * 2/ OLPOFRM, where ICPIL is the number of input clock cycles per line of the image data, ILPIFRM is the number of lines of the image data per frame of the image data, and OLPOFRM is the number of lines of the video signal per frame of said video signal, the value T is equal to ICPIL * ILPIFRM * 2 , the value A is equal to OLPOFRM, and the initial value I is equal to zero, and

in the second mode, the value T is equal to the number of input clock cycles per line of the video signal, the value A equal to one, and the initial value I is equal to zero.

38. The system of claim 29, wherein the output clock has frequency XF_o, X is an integer, and the frequency F_i is equal to $(T/A)F_o$, and wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to increase the Count value by the value A during each cycle of the input clock; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value T during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to reduce the Count value by the value T – A when the output signal indicates that the Count value has risen to a value greater than the value T, and wherein the output signal is said control signal.

39. The system of claim 29, wherein the output clock has frequency XF_o, X is an integer, and the frequency F_i is equal to $(T/A)F_o$, and wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to decrease the Count value by the value A during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + T, whenever the frame start signal is indicative of one of the frame start events, where X is a value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input

clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value T – A when the output signal indicates that the Count value has fallen to a value less than or equal to said value X, and wherein the output signal is said control signal.

40. The system of claim 29, wherein the output clock has frequency XF_o, X is an integer, and the frequency F_i is equal to $(T/A)F_o$, and wherein the first circuitry comprises:

an accumulator configured to store a Count value, and to decrease the Count value by the value A during each cycle of the input clock, wherein the accumulator is coupled to receive a frame start signal indicative of sequence of frame start events, and the accumulator is configured to set the Count value to an initial value I = X + T, whenever the frame start signal is indicative of one of the frame start events, where X is a value; and

a comparator coupled to the accumulator and configured to perform a comparison of the Count value with the value X during each cycle of the input clock and to generate an output signal indicative of the result of each said comparison,

wherein the accumulator is coupled to receive the output signal and configured to increase the Count value by the value T – A when the output signal indicates that the Count value has fallen to a value less than said value X, and wherein the output signal is said control signal.

41. The system of claim 29, wherein said system is a video game system also including:

a player-manipulated input device; and

a CPU coupled to the input device,

wherein the video game system operates in response to at least one input signal from the input device while a display device displays frames of the video signal, and wherein at least one of the input device and the CPU is configured to perform a pointing device function to determine at least one pixel of one of the frames of the video signal being displayed, from the at least one input signal.

42. The system of claim 41, wherein at least one of the input device and the CPU is coupled to the sync generator circuit to receive the synthesized sync pulses, and said at least one of the input device and the CPU is configured to perform the pointing device function in response to said synthesized sync pulses and said at least one input signal, but not in response to the output clock.

43. A method for generating a train of synthesized sync pulses in response to an input clock having frequency F_i, said method including the steps of:

(a) generating a control signal in response to the input clock in accordance with the Bresenham algorithm, such that the control signal is indicative of events having time-averaged frequency at least nearly equal to $(A/T)F_i$, where A and T are integer values, and such that accumulated error, between a first time from a first one to a last one of Z consecutive ones of said events and a second time equal to $ZT/(AF_i)$, never exceeds $1/F_i$; and

(b) generating the sync pulses in response to the control signal such that leading edges of the pulses occur at least nearly periodically, at said time-averaged frequency that is at least nearly equal to $(A/T)F_i$, and with accumulated error, between a third time from a first one to a last one of Z consecutive ones of said leading edges and the second time $ZT/(AF_i)$, that never exceeds $1/F_i$.

44. The method of claim 43, wherein step (a) including the steps of:

increasing a count value by the value A during each cycle of the input clock;

performing a comparison of the count value with the value T during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

reducing the count value by the value T – A when the control signal indicates that the count value has risen to a value greater than or equal to said value T.

45. The method of claim 44, wherein step (a) also includes the step of resetting the count value to an initial value in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

46. The method of claim 43, wherein step (a) including the steps of:

increasing a count value by the value A during each cycle of the input clock;

performing a comparison of the count value with the value T during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

reducing the count value by the value T – A when the control signal indicates that the count value has risen to a value greater than said value T.

47. The method of claim 43, wherein step (a) including the steps of:

(c) setting a count value to an initial value equal to X + T, where X is a value, in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

(d) after step (c), decreasing the count value by the value A during each cycle of the input clock;

(e) performing a comparison of the count value with the value X during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

(f) increasing the count value by the value T – A when the control signal indicates that the count value has fallen to a value less than or equal to said value X.

48. The method of claim 43, wherein step (a) including the steps of:

(c) setting a count value to an initial value equal to X + T, where X is a value, in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

(d) after step (c), decreasing the count value by the value A during each cycle of the input clock;

(e) performing a comparison of the count value with the value X during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

(f) increasing the count value by the value T – A when the control signal indicates that the count value has fallen to a value less than said value X.

49. A method of generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, said method including the steps of:

increasing a count value by an integer value D during each cycle of the input clock;

performing a comparison of the count value with a threshold value N during each cycle of the input clock to generate a control signal, wherein the control signal is indicative of the result of each said comparison;

reducing the count value by the threshold value N – D when the control signal indicates that the count value has risen to a value greater than or equal to said threshold value N; and

generating the sync pulses in response to said control signal.

50. The method of claim 49, also including the step of resetting the count value to an initial value in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

51. A method of generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, said method including the steps of:

increasing a count value by an integer value D during each cycle of the input clock;

performing a comparison of the count value with a threshold value N during each cycle of the input clock to generate a control signal, wherein the control signal is indicative of the result of each said comparison;

reducing the count value by the threshold value N – D when the control signal indicates that the count value has risen to a value greater than said threshold value N; and

generating the sync pulses in response to said control signal.

52. A method of generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, said method including the steps of:

(a) setting a count value to an initial value equal to X + N, where X is a value and N is an integer value, in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

(b) after step (a), decreasing the count value by an integer value D during each cycle of the input clock;

(c) performing a comparison of the count value with the value X during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

(d) increasing the count value by the value N – D when the control signal indicates that the count value has fallen to a value less than or equal to said value X.

53. A method of generating a train of synthesized sync pulses in accordance with the Bresenham algorithm in response to an input clock having frequency F_i, said method including the steps of:

(a) setting a count value to an initial value equal to X + N, where X is a value and N is an integer value, in response to a frame start signal, whenever the frame start signal is indicative of one of a sequence of frame start events.

(b) after step (a), decreasing the count value by an integer value D during each cycle of the input clock;

(c) performing a comparison of the count value with the value X during each cycle of the input clock to generate the control signal, wherein said control signal is indicative of the result of each said comparison; and

(d) increasing the count value by the value N – D when the control signal indicates that the count value has fallen to a value less than said value X.